User Guide and Interface Control Document

Contents

1 Overview

This document serves as a User Guide as well as Interface Control Document of the ELT-DPU-Z2CS – a Data Processing Unit (computer) designed for use in CubeSat-class, PC/104 mechanical form-factor compatible spacecraft. This document is applicable to ELT-DPU-Z2CS units in general. Each specific item of this type may be configured individually, and is tested individually, what is reflected in two additional documents shipped with every unit:

- ELT-DPU-Z2CS Configuration list
- ELT-DPU-Z2CS Output checklist

The Configuration list defines important options, such as what electrical interfaces are populated and what connector pins are connected to particular circuit nets.

2 Handling and safety

The ELT-DPU-Z2CS contains following substance registered as harmful according to RoHS/REACH:

- lead (Pb) contained in SnPb (60/40) solder.

For detailed materials list see Section 6.2.

Please follow your local regulations when handling and disposing off the device. Our recommendation is: do not eat and launch into space at earliest opportunity.

The unit is operated at low voltage (5V or 3.3V) and does not generate any higher voltage internally.

The unit is sensitive to electro-static discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

The unit is not intended for use in domestic environments. The unit may cause electromagnetic interference, for which appropriate measures must be taken.

Environmental conditions for safe operation and storage of the unit are specified in Section 6.1.

3 Bring-up and Quick start guide

The following order of steps shall be preserved when connecting and powering up the unit:

1. While powered-off, first establish a solid ground connection between ELT-DPU-Z2CS and the platform via H1/H2 connectors and their respective ground pins. The platform stands for: a spacecraft, flat-sat, test jig or laboratory power supply.
2. When EGSE is desired to operate system serial console, reset or JTAG programming, connect the EGSE via ELT-DPU-Z2CS's connector K3.
3. When used, connect the EGSE to a PC.
4. Optionally, connect the 1000BaseTx Ethernet dongle to connector K401, other end to a PC or Ethernet switch.
5. Make sure the platform's power supply is connected to the correct ELT-DPU-Z2CS's H1/H2 power supply pins as per the unit-specific Configuration list.
6. Switch the power on (nominally 3V3, unless the dual-powered i.e. 3V3 & 5V option was configured) at the platform.
7. ELT-DPU-Z2CS may be safely powered off anytime except when a FLASH/eMMC write is in progress.

For more example steps verifying basic functionality, such as test of the Ethernet and TCP/IP, initial OS login, CAN bus test and eMMC storage test, see the step-by-step procedure described in the Output checklist document supplied with every unit.

4 Unit description

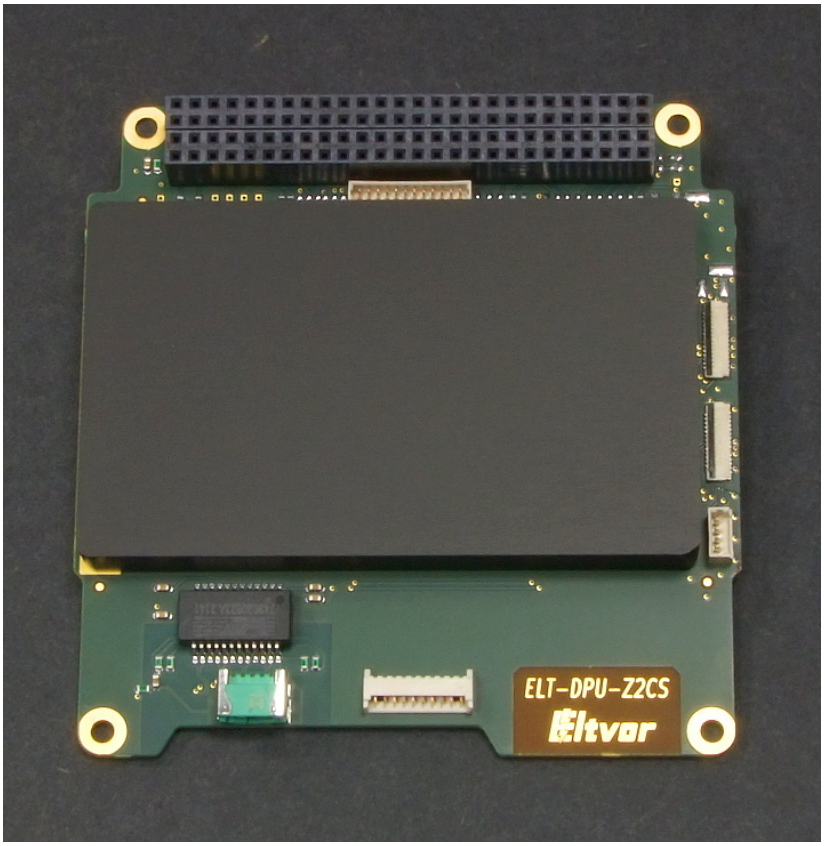

Figure 1: ELT-DPU-Z2CS photo

4.1 Features

4.1.1 Processing platform

SoC (CPU+FPGA):	- Xilinx Zynq 7z010 - or 7z020
RAM:	- 256MB DDR3 (case of 7z010 SoC) - 512MB DDR3 (case of 7z020 SoC)
PROM:	64MB QSPI FLASH 8GB eMMC mass storage

4.1.2 Interfaces

CAN	up to 1Mb/s
RS485	tested up to 3Mb/s, 32Mb/s theoretical
I2C	
Ethernet	1000BaseTx
USB	2.0 host
LVDS	14 pairs supports 2 cameras
UART	for SoC console
JTAG	for programming and in-system debugging

4.1.3 Power input

3V3	mandatory to power the SoC
5V	optional for camera powering
switches	3 independent power switches for: - 2 cameras - eMMC mass storage

5 Interfaces

5.1 Electrical – external interfaces

5.1.1 Grounding

Ground is permanently connected to the following pins of PC/104 connectors:

Pin(s)	Function
H2-23, H2-24, H2-29, H2-30, H2-32	gnd

The ground is also connected to the alternative bus connector K1 to the following pins:

Pin(s)	Function
K1-1, K1-6, K1-12	gnd

The ground may be also connected to two M3 mounting holes (out of total four M3 mounting holes) designated MNT1, MNT2. Each of these mounting holes is connected to ground via two 0603 footprints, which may be populated with a resistor, capacitor or 0 Ohm jumper. The selected grounding choice is reflected in the Configuration list.

5.1.2 Powering

5.1.2.1 Voltage The ELT-DPU-Z2CS operates normally from a single, 3.3V power supply. There is an optional setting, where the ELT-DPU-Z2CS provides power for one or two connected camera modules, and then the DPU requires two power rails, 3.3V & 5V. The selected option for specific item is reflected in Configuration list.

5.1.2.2 In-rush current Measured in-rush current when connected to hard 3.3V power supply over 0.22 Ω shunt resistance is plotted in Figure 2. The peak value of in-rush curent is 4.6A, the total charge of the transient is 264 μC.

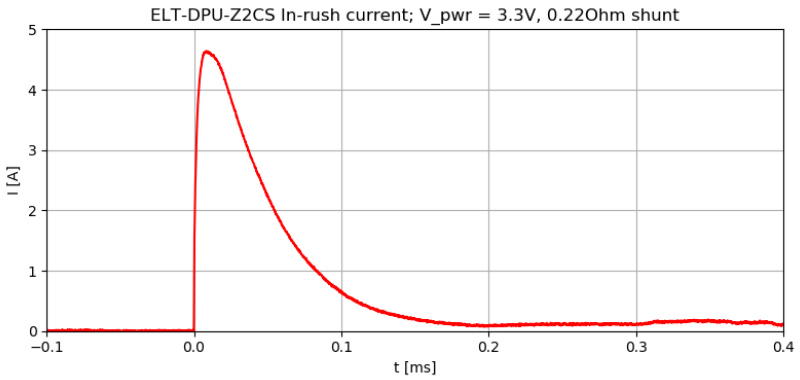

Figure 2: In-rush current

5.1.2.3 Power consumption Typical power consumption at room ambient temperature is recorded in the following Table 1.

Table 1: Power consumption

Conditions	Power consumption @3V3 [W]
booting	1.48
power consumption in operational state P_o:	
CPU idle	1.15
CPU 1 core full load (100% CPU)	1.32
CPU 2 cores full load (200% CPU)	1.49
additional consumption due to peripherals:	
Ethernet 1Gb/s up, idle	P_o+ 0.37
Ethernet 1Gb/s up, IP flood	P_o+ 0.43
eMMC on, burst read	P_o+ 0.18

The additional power consumption may be demanded by an FPGA fabric, when a non-trivial circuit is configured in. Use the Xilinx' power estimator tool to calculate power consumption for your specific design when FPGA subsystem is needed.

5.1.2.4 Protective components There are no diodes, transient voltage suppresors, parallel nor series resistors or other protection devices present at the power input, other than linear and switch-mode regulator integrated circuits.

5.1.3 Bus and communication interfaces

The main bus is expected to be connected via PC/104 connectors (H1, H2). All H1, H2 connections except ground are led via 0603 footprints/jumpers, so any of the listed connections may be disconnected. Several functions do support more alternative locations, such as power input. The actual configuration set during manufacturing is listed in Configuration list, and may be changed by (de)soldering according to Section 5.1.5.

Table 2: H1,H2:PC/104 bus

pin	function
H1-1	can0_l
H1-3	can0_h
H1-41, H2-21	i2c_sda
H1-43, H2-22	i2c_scl
H1-51, H1-52, H2-37, H2-42	pwr_3v3
H2-17	rs485_a
H2-18	rs485_b
H2-19	can1_h
H2-20	can1_l
H2-23, H2-24, H2-29, H2-30, H2-32	gnd
H2-52	time_pulse_3v3
Connector type: SSQ-126-03-G-D	

A reduced set of functions is present on the alternative bus connector K1. The connections here are fixed, no option jumpers. The pwr_5v power lines are applicable only in the case of dual-powered configuration.

Table 3: K1 connector

Pin(s)	Function
K1-1, K1-6, K1-12	gnd
K1-2, K1-3	pwr_5v
K1-4, K1-5	pwr_3v3
K1-7	can1_h
K1-8	can1_l
K1-9	rs485_a
K1-10	rs485_b
K1-11	time_pulse_3v3
Connector type: 53047-1210	

The 1000BaseTx Ethernet is connected via a dedicated connector K401:

Table 4: K401:1000BaseTx Ethernet

pin	function	comment
K401-1	eth_a_p	orange-white
K401-2	eth_a_n	orange
K401-3	eth_gnd	
K401-4	eth_b_p	green-white
K401-5	eth_b_n	green
K401-6	eth_d_p	brown-white
K401-7	eth_d_n	brown
K401-8	eth_gnd	
K401-9	eth_c_p	blue-white
K401-10	eth_c_n	blue
Connector type: G125-MH11005L7P		

The ELT-DPU-Z2CS is also equipped with a USB2.0 interface, by default configured as a USB host. The pwr_5v pin provides direct connection to the 5V power input, when the DPU is configured for dual-supply operation. Otherwise, the pin connects to 3V3 power input (which would be non-standard for USB-powered devices).

Table 5: K2:USB2.0 interface

Pin(s)	Function
K2-1	pwr_5v
K2-2	usb_d-
K2-3	usb_d+
K2-4	gnd
Connector type: 53047-0410	

5.1.3.1 Protective components and resistors There are no diodes, transient voltage suppresors, parallel nor series resistors or other protection devices present at the communication interface signal lines, other than respective bus driver integrated circuits. There are also no discrete pull-up or pull-down resistors. Optionally, the CAN buses and RS485 may be equipped with terminations resistors, specified in Configuration list.

5.1.4 Camera, LVDS and GPIO interfaces

The ELT-DPU-Z2CS provides two identical interfaces (K101, K102) primarily intended for use with Eltvor's camera modules, such as ELT-VCAM1M3 1.3Mpixel camera. Besides camera usage, each of these interfaces may be used as a generic 7-pair LVDS I/O (such as SpaceWire), plus 7 LVCMOS I/Os. The connector used is 29-pin, 0.3mm pitch mating with flex cable.

There are two type of electrical connection between K101, K102 and the SoC:

- LVDS – signals are led in 100 Ω balanced pairs. No additional components in the signal path. These pins are intended for use with LVDS 2V5 I/O standard. They may be used as a 2V5 single-ended I/O as well.
- LVCMOS – signals are connected individually, irrespective of differential pairs. Each I/O signal is connected to the SoC via 33 Ω series resistor. These pins are intended for use with LVCMOS 3V3 I/O standard.

The pin connections between K101, K102 and the SoC are listed in the following tables. Camera power lines cam_pwr_v1, cam_pwr_v2 are connected only in the case of dual-powered configuration.

Table 6: K101 pinout

K101 pin	I/O pin name	I/O pin location	I/O type
K101-1	B34_L15_N	U20	LVDS
K101-2	B34_L15_P	T20	LVDS
K101-3	B34_L1_N	T10	LVDS
K101-4	B34_L1_P	T11	LVDS
K101-5	B34_L4_N	V13	LVDS
K101-6	B34_L4_P	V12	LVDS
K101-7	B34_L18_N	W16	LVDS
K101-8	B34_L18_P	V16	LVDS
K101-9	B34_L19_N	R17	LVDS
K101-10	B34_L19_P	R16	LVDS
K101-11	B34_L11_N	U15	LVDS
K101-12	B34_L11_P	U14	LVDS
K101-13	B34_L16_N	W20	LVDS
K101-14	B34_L16_P	V20	LVDS
K101-16	B35_L15_N	F20	LVCMOS
K101-17	B35_L2_P	B19	LVCMOS
K101-18	B35_L4_P	D19	LVCMOS
K101-19	B35_L1_N	B20	LVCMOS
K101-20	B35_L15_P	F19	LVCMOS
K101-25	B35_L8_P	M17	LVCMOS
K101-26	B35_L19_P	H15	LVCMOS
Ground and power:			
K101-15	gnd		
K101-27	gnd		
K101-28	cam_pwr_v1		
K101-29	cam_pwr_v2		
Connector type: FH39-29S-03SHW10			

Table 7: K102 pinout

K101 pin	I/O pin name	I/O pin location	I/O type
K102-1	B34_L6_N	R14	LVDS
K102-2	B34_L6_P	P14	LVDS
K102-3	B34_L5_N	T15	LVDS
K102-4	B34_L5_P	T14	LVDS
K102-5	B34_L9_N	U17	LVDS
K102-6	B34_L9_P	T16	LVDS
K102-7	B34_L24_N	P16	LVDS
K102-8	B34_L24_P	P15	LVDS
K102-9	B34_L23_N	P18	LVDS
K102-10	B34_L23_P	N17	LVDS
K102-11	B34_L12_N	U19	LVDS
K102-12	B34_L12_P	U18	LVDS
K102-13	B34_L8_N	Y14	LVDS
K102-14	B34_L8_P	W14	LVDS
K102-16	B35_L12_P	K17	LVCMOS
K102-17	B35_L12_N	K18	LVCMOS
K102-18	B35_L24_P	K16	LVCMOS
K102-19	B35_L24_N	J16	LVCMOS
K102-20	B35_L16_P	G17	LVCMOS
K102-25	B35_L8_N	M18	LVCMOS
K102-26	B35_L19_N	G15	LVCMOS
Ground and power:			
K102-15	gnd		
K102-27	gnd		
K102-28	cam_pwr_v1		
K102-29	cam_pwr_v2		
Connector type: FH39-29S-03SHW10			

5.1.5 HW configuration

The HW configurable options are realised by soldering appropriate 0 Ohm jumpers, resistors and/or capacitors, according to the Configuration list. Some of the jumpers and/or other 0603-sized components are accessible to user without dismantling the shield, and their location on the circuit board is labeled in the following figure.

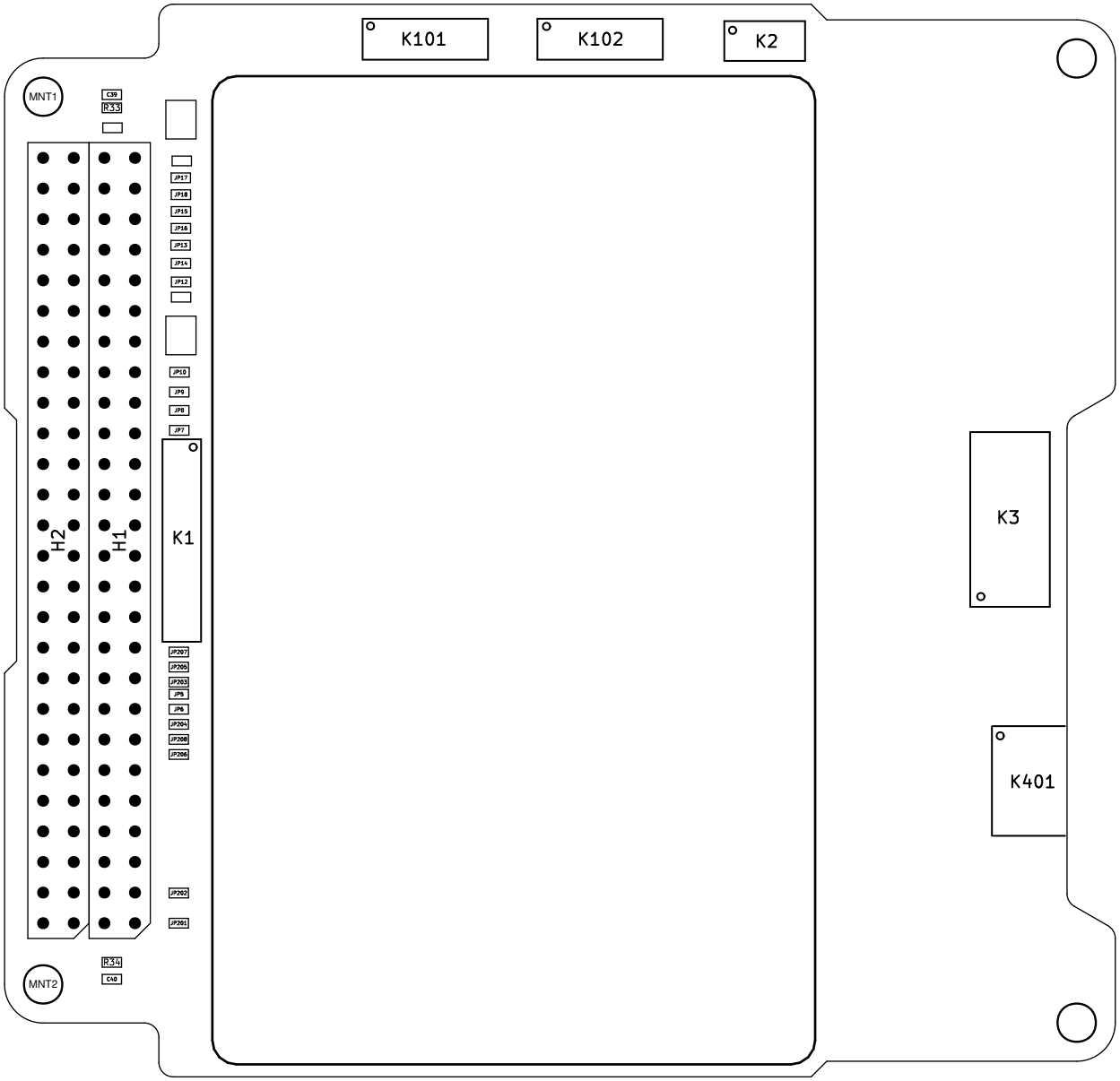

Figure 3: Assembly drawing

5.1.6 EGSE connection

The ELT-DPU-Z2CS exposes an umbilical connector (K3) intended for EGSE connection. The user shall access this connector via the provided ELT-DPU-Z2CS-EGSE, see Section 8.

5.2 Mechanical

5.2.1 Drawing

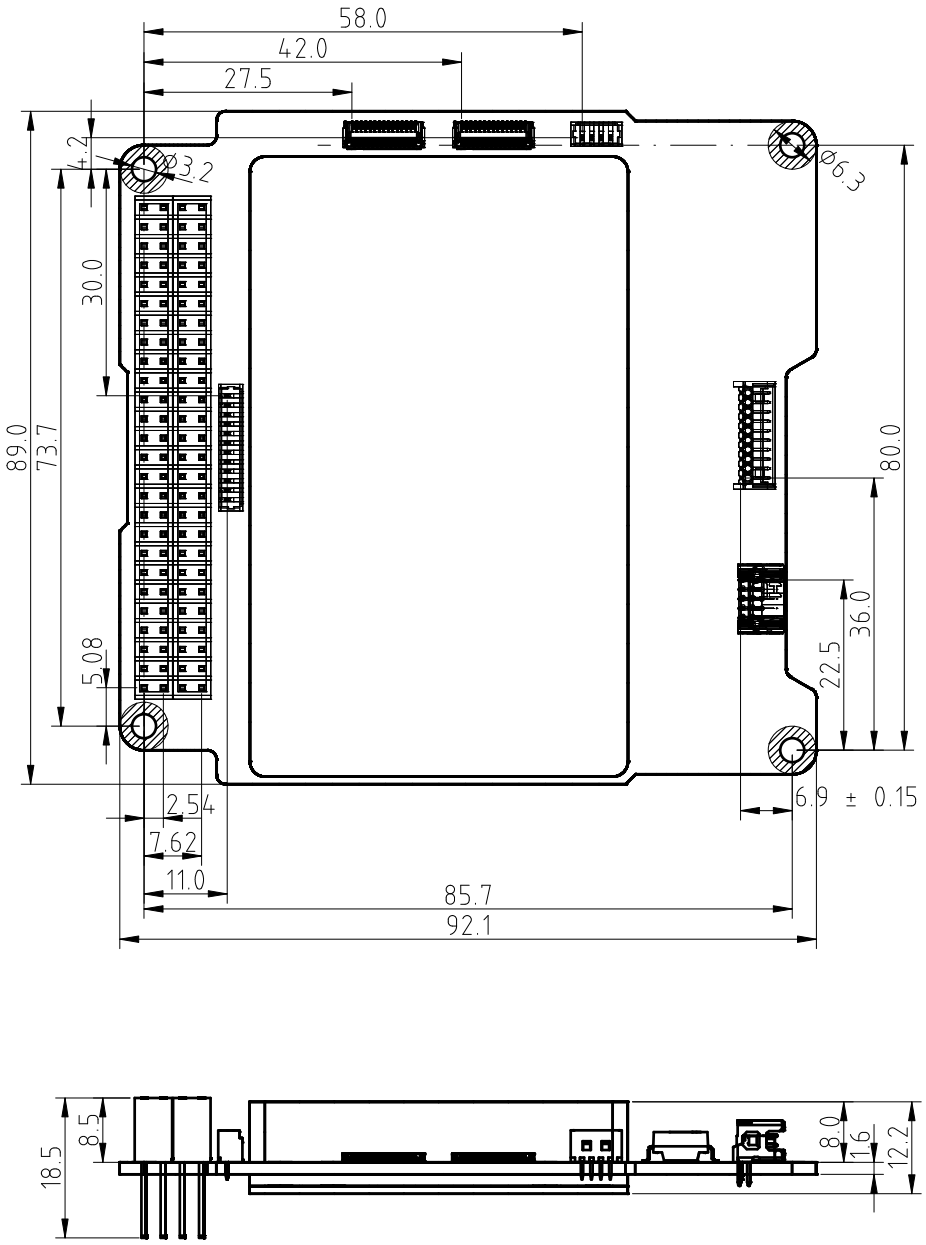

Figure 4: Drawing (scale 1:1)

5.2.2 3D model

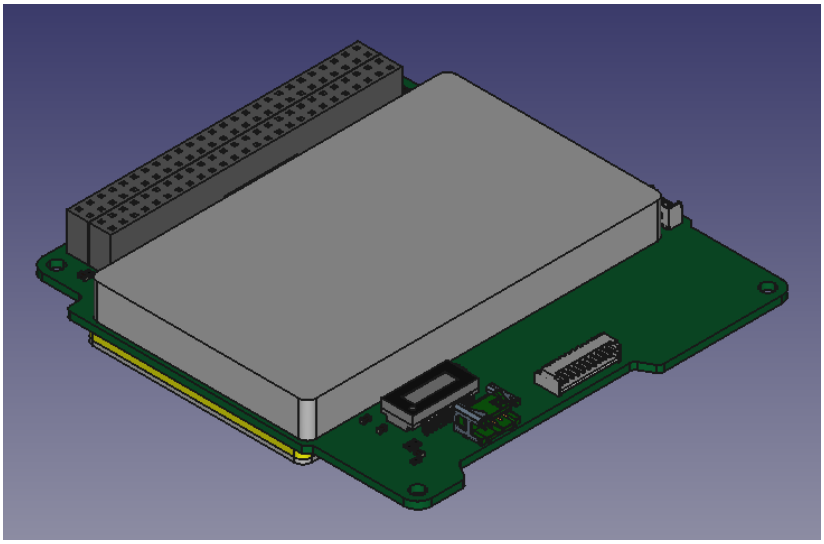

Figure 5: Isometric view of the CAD model; STEP model is delivered

5.2.3 Mass

The mass of ELT-DPU-Z2CS is: 118 g ±15 g.

5.3 Thermal

When no external powered devices such as cameras or USB device are connected to the ELT-DPU-Z2CS, practically all supplied power is dissipated in the DPU.

The thermal conductivity between the source of dissipated heat and the shld_top element of thermal-radiation shield is: 8.2 W/K.

The main DPU's pcb contains in average 0.12mm thick Cu.

6 General specifications

6.1 Environmental

6.1.1 Table of environmental parameters

Parameter	Details	min.	typ.	max.	Units
Total Ionising Dose	*Note 1		25		krad
Single-Event Effects	*Note 2				
Temperature (storage)		-40		+95	°C
Temperature (operational)	*Note 3	-40		+60	°C
Humidity				85	% RH
Shock	*Note 4				
Vibration	*Note 4				

6.1.2 Notes

1. The TID performance is based on a Co60 test performed on 3 pieces of the previous version of the DPU (ELT-DPU-Z1CS), which all failed around 25krad. The most susceptible part being the QSPI FLASH memory, the remaining SoC still operational. TBD: occurence of the first bit flip observed.
2. A cyclotron proton test has been performed on 1 piece of the previous version of the DPU (ELT-DPU-Z1CS). The results to be consolidated in the future revision of the document. No hard latch-ups observed.
3. The maximum temperature shall ensure the junction temperature (Tj) does not exceed 125°C, so depending on overall system-level thermal design and depending on duration of dissipated power duty factor, the upper bound shall be adjusted accordingly.

4. The previous version of the DPU (ELT-DPU-Z1CS) has been tested on a satellite-level in a mission VZLUSAT-2 (tested July—August 2020, launched January 2022). At the time being we do not possess the exact conditions and results of vibration and shock, will be hopefully amended in future revision of the document.

6.2 Material

The main materials constituting ELT-DPU-Z2CS are listed in the following table. The table does not list materials of the electrical connectors, which are listed in Section 5.1, and which in general contains plastic and metallic materials.

The table also does not list surface-mount electronic component, such as thin-film resistors, multilayer ceramic capacitors and integrated circuits in their plastic housings. The total mass of these components is <15g.

Material	Description	Usage
EN AW 5754	aluminium alloy	thermal-radiation shield - shld_top - shld_bot
Rogers RO4350B	ceramic pcb substrate	shield insulation spacer - shld_insl
Ventec VT-47	pcb substrate	main pcb
Electra EMP-110	pcb mask	main pcb
SnPb 60/40	solder	main pcb
A4 stainless steel	screws	- 8x M3x8 screw - 2x M2x8 screw
Loctite 243	1-component dimethacrylate ester	securing all screw threads
3M 2216	2-component epoxy	securing 8x M3 screw heads

7 Developer's guide

7.1 Introduction

The core of the ELT-DPU-Z2CS is a combined CPU+FPGA System-on-Chip (SoC), Xilinx Zynq 7000 series. The functional description of this SoC is given in Xilinx' UG585: Zynq-7000 Technical Reference Manual.

The other members of chipset and functions specific to ELT-DPU-Z2CS and their internal connections to the SoC are described in this chapter. From the user perspective, the SoC is composed of two main subsystems:

- CPU and hard-wired peripherals, together known as PS (Processing System);
- FPGA fabric, known as PL (Programmable Logic).

The functions of ELT-DPU-Z2CS are controlled by either PS, or PL, or both. Some of the I/O pins are connected to PL only, such as power switches or time pulse input, some of them are connected to both PS and PL, such as CAN bus signals, and some are connected to PS only, such as eMMC. In case a function driven solely by the PL is needed, the user has to initialise the PL with appropriate FPGA bitstream. The I/O pins accessible by PS are designated with a *MIO+number* identifier, listed in Section 7.4.2, which corresponds to the internal SoC pin to be used and selected by an I/O multiplexer.

7.2 Memory

7.2.1 QSPI FLASH

The primary non-volatile memory of the ELT-DPU-Z2CS is a QSPI FLASH, 64MB. By default, the SoC is configured to boot from this QSPI FLASH.

7.2.2 eMMC

The eMMC is operated on single, 3V3 power supply ("no-1V8" mode). eMMC is connected to MIO pins of Bank 13, see signals mmc_* in Section 7.4.2.

The configuration of the SoC boot mode may be changed to boot from eMMC. Also, the EGSE may change the boot mode to boot from eMMC. In that case however it is necessary to configure the default eMMC power switch status, see the description in Configuration list.

7.3 Power switches

There are three power switches in the ELT-DPU-Z2CS, operated optionally by PL I/O pins. One is for switching on the eMMC storage (mmc_pwr_on), and other two (cam*_pwr_on) are able to switch power supplied to two external cameras (valid only with dual-supply option). The switch control signal is in positive logic, i.e. writing 0 means off, writing 1 means on.

7.4 Internal I/O connections

7.4.1 I/O bank voltages

Bank	Voltage	Note
Bank 34	2V5	1V8 may be configured on request
Bank 35	3V3	
Bank 13	3V3	

7.4.2 I/O pin assignment

Signal	I/O pin name	MIO identifier	I/O pin location	Note
eMMC				
mmc_clk	B13_L16_P	MIO40	W10	
mmc_cmd	B13_L16_N	MIO41	W9	
mmc_d0	B13_L18_P	MIO42	W11	
mmc_d1	B13_L18_N	MIO43	Y11	
mmc_d2	B13_L14_P	MIO44	Y9	
mmc_d3	B13_L14_N	MIO45	Y8	
Console UART				
uart_tx	B13_L19_N	MIO47	U5	from DPU
uart_rx	B13_L19_P	MIO46	T5	to DPU
Power switches				
mmc_pwr_on	B35_L7_P		M19	
cam0_pwr_on	B35_L1_P		C20	Camera 0 power
cam1_pwr_on	B35_L16_N		G18	Camera 1 power
RS485				
rs485_rxd	B35_L5_P		E18	Rx from bus
rs485_txd	B35_L3_P		E17	Tx to bus
rs485_txe	B35_L5_N		E19	1=Tx enable
Time pulse / General purpose input				
time_pulse	B35_L7_N		M20	
CAN0				
can0_tx	B13_L12_N	MIO51	U10	mutually exclusive options
	B35_L10_P		K19	
can0_rx	B13_L12_P	MIO50	T9	
	B35_L10_N		J19	
CAN1				
can1_tx	B13_L11_P	MIO48	U7	mutually exclusive options
	B35_L4_N		D20	
can1_rx	B13_L11_N	MIO49	V7	
	B35_L2_N		A20	

The USB host interface is connected to PS pins corresponding to USB0.

8 EGSE

8.1 Contents

In order to facilitate programming, debugging and ground support of the ELT-DPU-Z2CS, the ELT-DPU-Z2CS-EGSE is provided, consisting of the following items:

- ELT-Z2CS-DPU-EGSE
  - containing a ELT-USB2232H module mounted on top
- 10wire cable to connect EGSE to DPU
- Gecko G125 to RJ45 Ethernet dongle

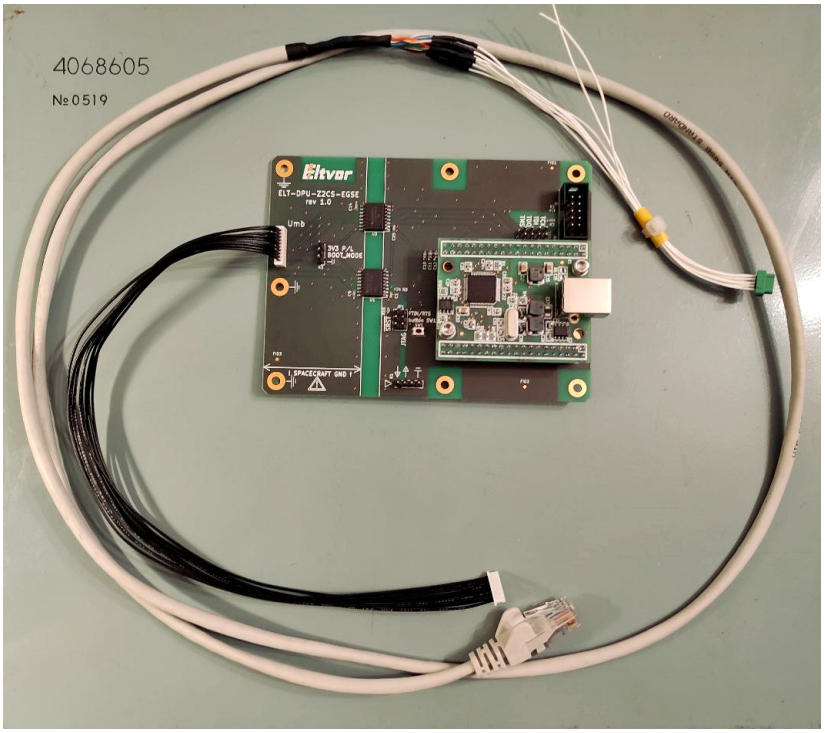

Figure 6: ELT-Z2CS-DPU-EGSE photo

8.2 Features

The EGSE provides following functions, galvanically isolated, controlled via USB from EGSE PC:

- Console UART
- JTAG for initial programming and in-system debugging
- System reset

8.3 Connectors and jumpers

The EGSE is equipped with the following electrical connectors:

- Umb – this connector is to be connected to the ELT-DPU-Z2CS via the supplied 10pin cable
- USB type B – to be connected to EGSE PC
- K6 – optional external JTAG connection, normally unused
- K1 – optional external UART, normally unused

The EGSE may be configured using 2.54mm jumpers of following functions:

- K5 – may be used to override SoC boot mode. The center pin is BOOT_MODE, may be connected to ground, to 3V3 P/L, or left unconnected. The default is unconnected.
- JP1 – reset (SRST) source. The JP1 allows to select the source of system reset (SRST): RTS pin of the FTDI UART, JTAG pin (K6-6) or SW1 pushbutton. Configuring RTS or JTAG allows for unmanned reset of the DPU.
- TCK, TDI, TDO, TMS – jumpers connecting the FTDI board to the DPU JTAG pins. These jumpers shall be in place when K6 is unused, which is default.

8.4 Usage

The safe order of connecting of the EGSE to the ELT-DPU-Z2CS is described in Section 3. When connecting to a host PC via USB2.0, the EGSE appears as a FTDI FT2232H chip. The EGSE functions are mapped to FT2232H functions as follows:

- Console UART – FT2232H port B (second interface, e.g. under Linux /dev/ttyUSB1)
- JTAG – FT2232H port A (first interface, MPSSE mode)

The JTAG may be used with Xilinx tools via intermediate server SW xvcd-ft2232h.
The console UART needs no special SW, just a terminal emulator. Nominal UART settings are 115200 bps, 8N1.

8.4.1 External JTAG

Normally, the JTAG is operated via the ELT-USB2232H module. In a specific case when a different JTAG adaptor is to be connected to the DPU, it is possible to connect an external JTAG via the K6 connector. Prior to this, the four jumpers (TCK, TDI, TDO, TMS) have to be disconnected (open). The voltage standard of JTAG at connector K6 is fixed to 3V3, and its pinout is listed in the following table.

Table 8: K6:External JTAG interface

Pin	Function	Pin	Function
K6-1	TCK	K6-2	NC
K6-3	TDO	K6-4	3V3
K6-5	TMS	K6-6	/SRST
K6-7	NC	K6-8	NC
K6-9	TDI	K6-10	GND
Connector type: DS1013-10SSIB1-B-0			

8.4.2 Handling and safety

The safety and handling of EGSE follows the same rules and conditions as specified for the ELT-DPU-Z2CS in Section 2.